16-BIT, 4-MSPS, PSEUDO-BIPOLAR, FULLY DIFFERENTIAL INPUT, MICROPOWER SAMPLING ANALOG-TO-DIGITAL CONVERTER WITH PARALLEL INTERFACE, REFERENCE

FEATURES

- **Fully Differential Input with Pseudo-Bipolar Input Range -4 V to +4 V**
- **16-Bit NMC at 4 MSPS**
- **1 LSB INL Typ**
- **92dB SNR, -102dB THD Typ with 100-kHz Input**
- **Internal 4.096-V Reference and Reference Buffer**
- **REFIN/2 Available for Setting Analog Input Common-Mode Voltage**
- **Zero Latency**
- **High-Speed Parallel Interface**
- **Single Supply Operation Capability**
- **Low Power: 155 mW at 4 MHz Typ, Flexible Power-Down Scheme**
- **Pin-Out Similar to ADS8412/8402**
- **48-Pin 9×9 TQFP Package**

APPLICATIONS

- **DWDM**
- **Instrumentation**
- **High-Speed, High-Resolution, Zero Latency Data Acquisition Systems**
- **Transducer Interface**
- **Medical Instruments**
- **Spectrum Analysis**
- **ATE**

DESCRIPTION

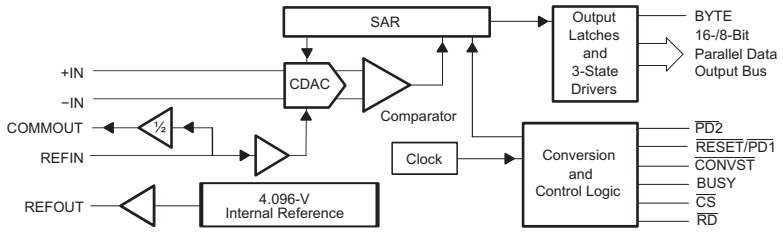
The ADS8422 is a 16-bit, 4-MHz A/D converter with an internal 4.096-V reference. The device includes a 16-bit capacitor-based multi-bit SAR A/D converter with inherent sample and hold. This converter includes a full 16-bit interface and an 8-bit option where data is read using two 8-bit read cycles if necessary.

The ADS8422 has a fully differential, pseudo-bipolar input. It is available in a 48-lead TQFP package and is characterized over the industrial -40°C to +85°C temperature range.

HIGH-SPEED SAR CONVERTER FAMILY(1)

TYPE/SPEED	500 kHz	~600 kHz	750 kHz	1 MHz	1.25 MHz	2 MHz	3 MHz	4MHz
18-Bit Pseudo-Diff	ADS8383	ADS8381		ADS8481				
		ADS8380 (s)						
18-Bit Pseudo-Bipolar, Fully Diff		ADS8382 (s)		ADS8482				
16-Bit Pseudo-Diff		ADS8370 (s)	ADS8371	ADS8471	ADS8401	ADS8411		
	ADS8327/28 (s)	ADS8372 (s)		ADS8329/30 (s)	ADS8405	ADS8410 (s)		
16-Bit Pseudo-Bipolar, Fully Diff				ADS8472	ADS8402	ADS8412		ADS8422
					ADS8406	ADS8413 (s)		
14-Bit Pseudo-Diff					ADS7890 (s)		ADS7891	
12-Bit Pseudo-Diff				ADS7886		ADS7883		ADS7881

(1) S: Serial



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QTY.
ADS8422I	±6	±2	15	9×9 48-Pin TQFP	PFB	–40°C to 85°C	ADS8422IPFBT	Small tape and reel 250
							ADS8422IPFBR	Tape and reel 1000
ADS8422IB	±2	+1.5/-1	16	9×9 48-Pin TQFP	PFB	–40°C to 85°C	ADS8422IBPFBT	Small tape and reel 250
							ADS8422IBPFBR	Tape and reel 1000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
	Voltage	+IN to AGND	–0.4 to +VA + 0.1	V
		–IN to AGND	–0.4 to +VA + 0.1	V
		+VA to AGND	–0.3 to 7	V
		+VBD to BDGND	–0.3 to 7	V
	Digital input voltage to BDGND		–0.3 to +VBD + 0.3	V
	Digital output voltage to BDGND		–0.3 to +VBD + 0.3	V
T_A	Operating free-air temperature range		–40 to 85	°C
T_{stg}	Storage temperature range		–65 to 150	°C
	Junction temperature (T_J max)		150	°C
	TQFP 48-pin package	Power dissipation	$(T_J Max – T_A)/\theta_{JA}$	
		θ_{JA} thermal impedance	86	°C/W
	Lead temperature, soldering	Vapor phase (60 sec)	215	°C
		Infrared (15 sec)	220	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SPECIFICATIONS

T_A = –40°C to 85°C, +VA = 5 V, +VAREG = 5 V to 3 V, +VBD = 5 V to 2.7 V, f_{SAMPLE} = 4 MSPS, V_{ref} = 4.096 V (measured with internal reference buffer) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
Full-scale input voltage (1)		+IN – (–IN)	$–V_{ref}$		V_{ref}	V
Absolute input voltage		+IN	–0.2		V_{ref} + 0.2	V
		–IN	–0.2		V_{ref} + 0.2	
Common-mode input range			$(V_{ref})/2$ – 0.2	$(V_{ref})/2$	$(V_{ref})/2$ + 0.2	V
Input capacitance				30		pF
Input leakage current					1	nA
SYSTEM PERFORMANCE						
Resolution				16		Bits
No missing codes	ADS8422I		15			Bits
	ADS8422IB		16			
Integral linearity (2)(3)	ADS8422I		–6	±2	6	LSB (16 bit) (2)
	ADS8422IB		–2	±1	2	
Differential linearity	ADS8422I		–2	±0.7	2	LSB (16 bit)
	ADS8422IB		–1	±0.7	1.5	
Offset error			–0.5	±0.25	0.5	mV
Offset error drift				±0.2		ppm/°C
Gain error (4)(5)		V_{ref} = 4.096 V	–0.1	±0.05	0.1	%FS
Gain error drift		V_{ref} = 4.096 V		±2		ppm/°C
Common-mode rejection ratio		At dc		81		dB
		At code 0000h with [+IN + (–IN)]/2 = 512 mV_{pp} at 500 kHz,		78		
Noise		At 0000h output code		40		µV RMS
Power supply rejection ratio		At 8000h output code		78		dB
SAMPLING DYNAMICS						
Conversion time					0.180	µs
Acquisition time			0.070			µs
Throughput rate					4	MHz
Aperture delay				3		ns
Aperture jitter				7		ps RMS
Step response				70		ns
Overvoltage recovery				140		ns

(1) Ideal input span, does not include gain or offset error.
(2) LSB means least significant bit and is equal to $2V_{REF}/65536$.
(3) This is endpoint INL, not best fit.
(4) Measured relative to an ideal full-scale input [+IN – (–IN)] of 8.192 V.
(5) This specification does not include the internal reference voltage error and drift.

SPECIFICATIONS (Continued)

T_A = –40°C to 85°C, +VA = 5 V, +VAREG = 5.25 V to 3 V, +VBD = 5 V to 2.7 V, f_{SAMPLE} = 4 MSPS, V_{ref} = 4.096 V (measured with internal reference buffer) (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS						
Total harmonic distortion (THD)(1)	V_{IN} = 8 V_{pp}	10 kHz		–114		dB
		100 kHz		–102		
		500 kHz		–100		
Signal to noise ratio (SNR)	V_{IN} = 8 V_{pp}	10 kHz		93		dB
		100 kHz		92		
		500 kHz		90		
Signal to noise + distortion (SINAD)	V_{IN} = 8 V_{pp}	10 kHz		92.5		dB
		100 kHz		91.5		
		500 kHz		89.5		
Spurious free dynamic range (SFDR)	V_{IN} = 8 V_{pp}	10 kHz		116		dB
		100 kHz		109		
		500 kHz		106		
–3dB Small signal bandwidth				30		MHz
Maximum input frequency, $f_{i(max)}$(2)	V_{IN} = 8 V_{pp}		2			MHz
VOLTAGE REFERENCE INPUT						
Reference voltage at REFIN, V_{ref}			3.9	4.096	4.15	V
Reference resistance				1000		MΩ
INTERNAL REFERENCE OUTPUT						
Internal reference start-up time	From 95% (+VA), with 1-µF capacitor on REFOUT				25	ms
Reference voltage range, V_{ref}	I_O = 0, T_A = 25°C		4.088	4.096	4.104	V
Source current	Static load				10	µA
Line regulation	+VA = 4.75 V to 5.25 V			±1		mV
Drift	I_O = 0			±6		PPM/°C
ANALOG COMMON-MODE, PIN 3						
Output voltage range	I_O = 0		V_{REF}/2 - 0.016	V_{REF}/2	V_{REF}/2 + 0.016	V
Source current	Static load			200		µA

(1) Calculated on the first nine harmonics of the input frequency.
(2) ADC Sampling circuit is optimized to accept inputs until Nyquist frequency. Dynamic performance may degrade rapidly above $f_{i(max)}$.

SPECIFICATIONS (Continued)

T_A = –40°C to 85°C, +VA = 5 V, +VAREG = 5 V to 3 V, +VBD = 5 V to 2.7 V, f_{SAMPLE} = 4 MSPS, V_{ref} = 4.096 V (measured with internal reference buffer) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT						
Logic family – CMOS						
Logic level	V_{IH}	I_{IH} = 5 µA	0.75×(+VBD)		+VBD + 0.3	V
	V_{IL}	I_{IL} = 5 µA	–0.3		0.8	
	V_{OH}	I_{OH} = 2 TTL loads	+VBD – 0.6			
	V_{OL}	I_{OL} = 2 TTL loads			0.4	
Data format – Twos complement						
POWER SUPPLY REQUIREMENTS						
Power supply voltage	+VA		4.75	5	5.25	V
	+VAREG		2.85	3.0	5.25	
	+VBD		2.7	3.0	5.25	
Supply current	+VA	+VA = 5 V, $\overline{PD1}$ = 1, $\overline{PD2}$ = 1		24	27	mA
	+VAREG	+VAREG = 5 V, $\overline{PD1}$ = 1, $\overline{PD2}$ = 1		12	14	mA
		+VAREG = 3 V, $\overline{PD1}$ = 1, $\overline{PD2}$ = 1		12	14	
	+VBD(1)	+VBD = 3 V, 10 pF/pin		0.55		mA
		+VBD = 5 V, 20 pF/pin		1.8		
POWER DOWN(2)						
Supply current	+VA	$\overline{PD1}$ = 0, $\overline{PD2}$ = 1, +VA = 5 V		2.5	3.4	mA
	+VAREG			5		µA
Power					17	mW
Power-up time		($\overline{PD1}$, $\overline{PD2}$) : (0,1) → (1,1)			5	µs
Supply current	+VA	$\overline{PD1}$ = 0, $\overline{PD2}$ = 0		5		µ A
	+VAREG			5		
Power				40		µW
Power-up time		($\overline{PD1}$, $\overline{PD2}$) : (0,0) → (1,1) , 1-µF Storage capacitor from REFOUT to AGND			25	ms
TEMPERATURE RANGE						
Operating free-air			–40		85	°C

(1) This includes the current required for charging the external load capacitance on the digital outputs and is measured with four digital outputs toggling at the same time.
(2) ($\overline{PD_1}$, $\overline{PD_2}$) = (1,0) is reserved. Do not use this power-down pins combination.

TIMING CHARACTERISTICS FROM DIGITAL INPUTS

All specifications typical at –40°C to 85°C, +VBD = 2.7 V to 5.25 V [(1)(2)]

PARAMETER			MIN	TYP	MAX	UNIT
CONVERSION AND ACQUISITION						
$t_{(ACQ)}$	Acquisition time, internal to device, not externally visible		70			ns
t_{w1}	Pulse duration, $\overline{CONVST}$ low		20			ns
t_{w2}	Pulse duration, $\overline{CONVST}$ high		100			ns
t_{p1}	Period, $\overline{CONVST}$		250			ns
t_{q1}	Quiet time, last toggle of interface input signals during acquisition before $\overline{CONVST}$ falling [(3)]		30			ns
t_{q2}	Quiet time, $\overline{CONVST}$ falling to first toggle of interface input signals [(3)]		10			ns
POWER DOWN						
t_{w3}	Pulse duration	$\overline{PD1}$ low for only ADC reset (no powerdown)	20		500	ns
		$\overline{PD1}$ low for ADC reset and also ADC powerdown	1500			
		$\overline{PD2}$ low pulse duration for REFOUT and COMMOUT buffers powerdown	1500			
	Pulse duration, all others unspecified		10			ns

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of V_{DD}) and timed from after 90% of transition.
(2) All digital output signals loaded with 10-pF capacitors at +VBD = 2.7 V and 20-pF capacitor at +VBD = 5.25 V and timed to reaching 90% of transition.
(3) Quiet time zones are for meeting performance and not functionality.

TIMING CHARACTERISTICS OF DIGITAL OUTPUTS

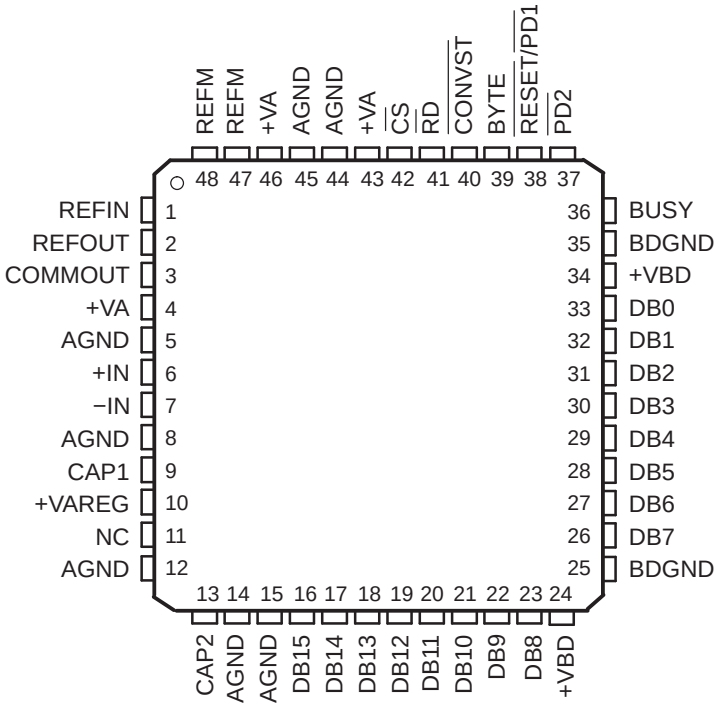
All specifications typical at –40°C to 85°C, +VBD = 2.7 V to 5.25 V [(1)(2)]

PARAMETER		MIN	TYP	MAX	UNIT
CONVERSION AND ACQUISITION					
$t_{(CONV)}$	Conversion time, internal to device, not externally visible			180	ns
t_{d1}	Delay time, $\overline{CONVST}$ fall to conversion start (aperture delay)		3		ns
DATA READ OPERATION					
t_{d2}	Delay time, $\overline{CONVST}$ low to data valid if $\overline{CS} = \overline{RD} = 0$			225	ns
t_{d3}	Delay time, data valid to BUSY low if $\overline{CS} = \overline{RD} = 0$	5			ns
t_{d4}	Delay time, $\overline{RD}$ (or $\overline{CS}$) low to data valid			17	ns
t_{d5}	Delay time, BYTE toggle to data valid			20	ns
t_{d6}	Delay time, data three-state after $\overline{RD}$ (or $\overline{CS}$) high			12	ns
POWER DOWN					
t_{d7}	Delay time, $\overline{PD1}$ low to BUSY rising			20	ns
t_{d8}	Delay time, $\overline{PD1}$ high to device operational (with $\overline{PD2}$ held high)			5	µs
	Delay time, $\overline{PD2}$ high to REFOUT/COMMOUT valid			25	ms
	Delay time, power up (after AV_{DD} = 4.75 V)			25	ms
t_{d9}	Delay time, data three-state after $\overline{PD1}$ low			1.5	µs

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of V_{DD}) and timed from after 90% of transition.
(2) All digital output signals loaded with 10-pF capacitors at +VBD = 2.7 V and 20-pF capacitor at +VBD = 5.25 V and timed to reaching 90% of transition.

PIN ASSIGNMENTS

PFB Package
(Top View)



A. NC - No connection

B. Pins 9 and 13 are internally regulated 3-V outputs and are externally to be connected to decoupling capacitors only.

C. +VAREG can be connected to a 3-V to 5-V supply.

D. Pin 3 outputs REFIN/2

E. Pin 38 can be used for ADC powerdown and pin 37 for analog output powerdown.

TERMINAL FUNCTIONS

NAME	NO	I/O	DESCRIPTION		
AGND	5, 8, 12, 14, 15, 44, 45	–	Analog ground		
BDGND	25, 35	–	Digital ground for bus interface digital supply		
BUSY	36	O	Status output. High when a conversion is in progress.		
BYTE	39	I	Byte select input. Used for 8-bit bus reading. 0: No fold back 1: Low byte D[7:0] of the 16 most significant bits is folded back to high byte of the 16 most significant pins DB[15:8].		
COMMOUT	3	O	This pin outputs REFIN/2 and can be used to set the common-mode voltage of the differential analog input, (+IN + –IN)/2.		
$\overline{\text{CONVST}}$	40	I	Convert start. This input is low true and can act independent of the $\overline{\text{CS}}$ input.		
$\overline{\text{CS}}$	42	I	Chip select.		
CAP1, CAP2	9, 13	O	Decoupling of internally generated 3-V supply. Add 1-µF capacitor from these pins to AGND.		
Data Bus			8-BIT BUS		16-BIT BUS
			BYTE = 0	BYTE = 1	BYTE = 0
DB15	16	O	D15 (MSB)	D7	D15 (MSB)
DB14	17	O	D14	D6	D14
DB13	18	O	D13	D5	D13
DB12	19	O	D12	D4	D12
DB11	20	O	D11	D3	D11
DB10	21	O	D10	D2	D10

TERMINAL FUNCTIONS (continued)

NAME	NO	I/O	DESCRIPTION		
DB9	22	O	D9	D1	D9
DB8	23	O	D8	D0 (LSB)	D8
DB7	26	O	D7	All ones	D7
DB6	27	O	D6	All ones	D6
DB5	28	O	D5	All ones	D5
DB4	29	O	D4	All ones	D4
DB3	30	O	D3	All ones	D3
DB2	31	O	D2	All ones	D2
DB1	32	O	D1	All ones	D1
DB0	33	O	D0 (LSB)	All ones	D0 (LSB)
–IN	7	I	Inverting input channel		
+IN	6	I	Noninverting input channel		
NC	11	–	No connection		
$\overline{PD2}$	37	I	Low true signal. A logic low longer than 1.5 µs applied to this pin powers down only the analog outputs that include REFOUT and COMMOUT. (NOTE: The combination $\overline{PD1}$ = 1, $\overline{PD2}$ = 0 is reserved. Do not use this combination.)		
REFIN	1	I	Reference input. Add 0.1-µF decoupling capacitor between REFIN and REFM.		
REFOUT	2	O	Reference output. Add 1-µF capacitor between the REFOUT pin and REFM pin when internal reference is used.		
REFM	47, 48	I	Reference ground		
$\overline{RESET}$/$\overline{PD1}$	38	I	Low true signal. A low pulse applied to this pin resets the ADC; the ongoing conversion is aborted. A low pulse shorter than 0.5 µs only resets, and one longer than 1.5 µs resets and also powers down the ADC. Note that analog outputs REFOUT and COMMOUT can be powered down by $\overline{PD2}$, if necessary.		
$\overline{RD}$	41	I	Synchronization pulse for the parallel output.		
+VA	4, 46	–	Analog power supplies, 4.75 V to 5.25 VDC		
+VAREG	10	–	Regulator supply, 2.85 V to 5.25 VDC		
+VBD	24, 34	–	Digital power supply for bus		

TYPICAL CHARACTERISTICS

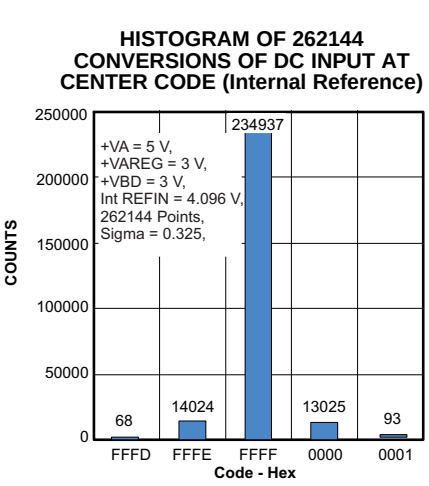


Figure 1.

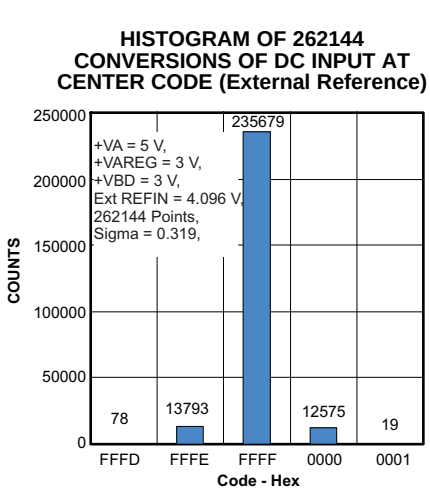


Figure 2.

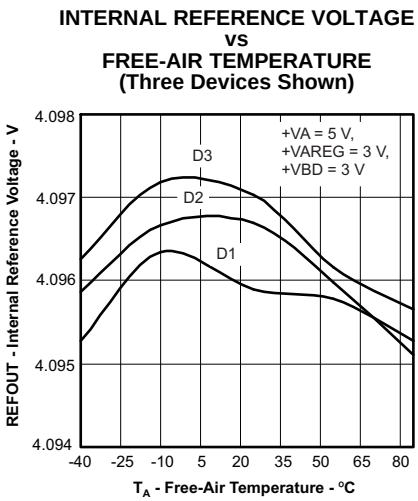


Figure 3.

TYPICAL CHARACTERISTICS (continued)

OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

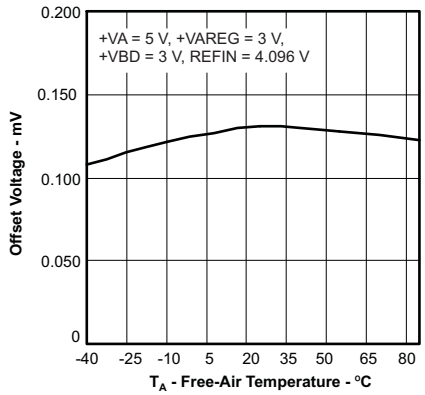


Figure 4.

GAIN ERROR vs FREE-AIR TEMPERATURE

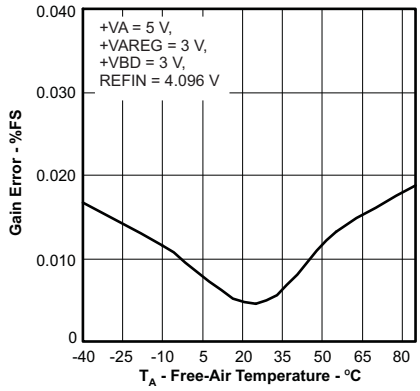


Figure 5.

SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

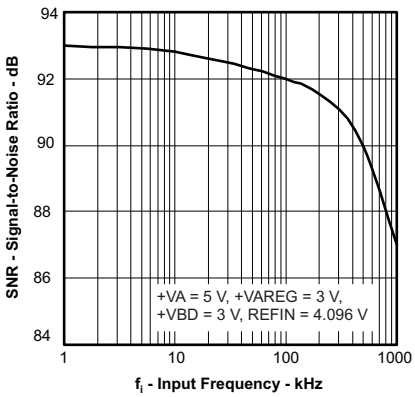


Figure 6.

SIGNAL-TO-NOISE + DISTORTION vs INPUT FREQUENCY

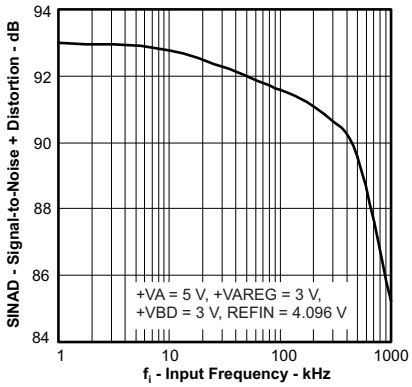


Figure 7.

EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

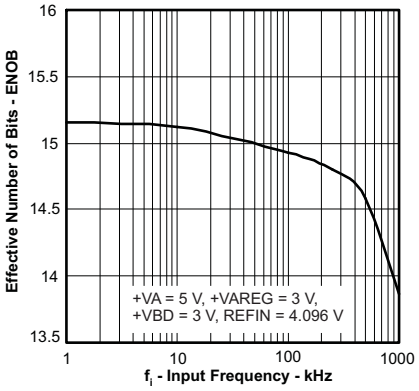


Figure 8.

SIGNAL-TO-NOISE RATIO vs FREE-AIR TEMPERATURE

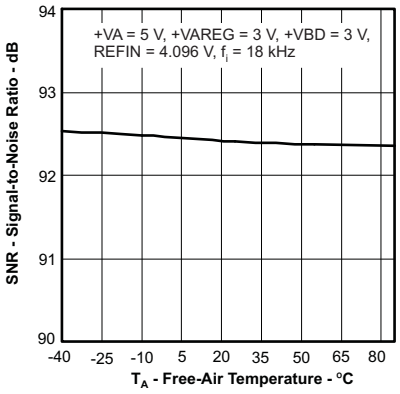


Figure 9.

TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

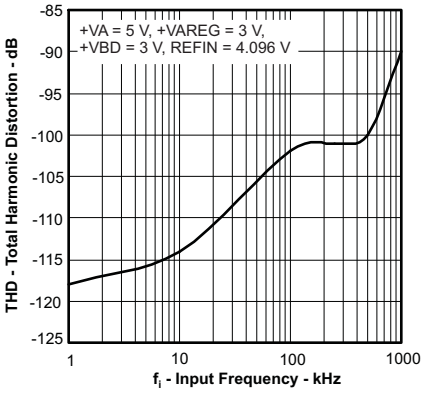


Figure 10.

SPURIOUS FREE DYNAMIC RANGE vs INPUT FREQUENCY

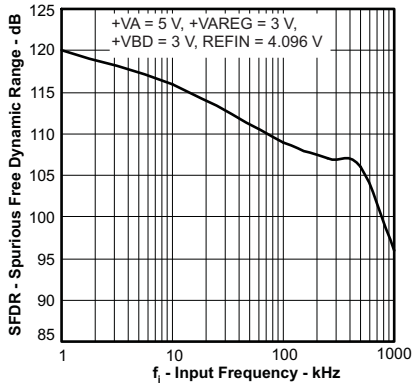


Figure 11.

TOTAL HARMONIC DISTORTION vs FREE-AIR TEMPERATURE

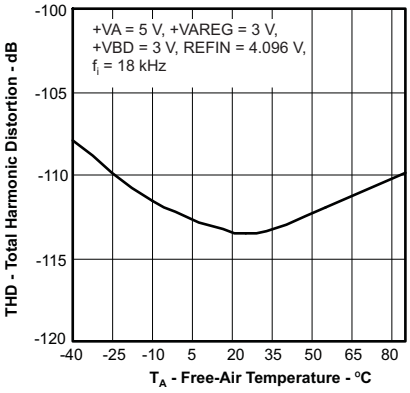


Figure 12.

TYPICAL CHARACTERISTICS (continued)

POWER DISSIPATION vs THROUGHPUT

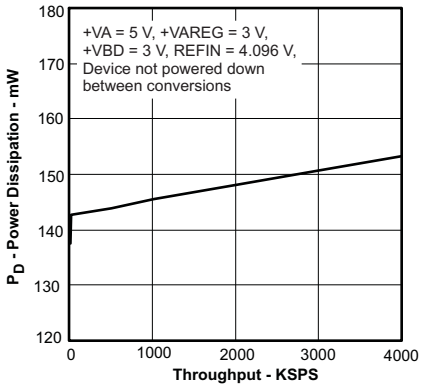


Figure 13.

+VAREG CURRENT vs THROUGHPUT

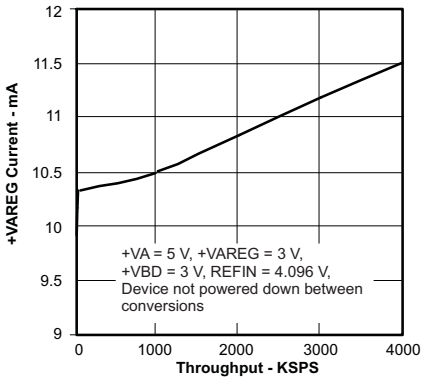


Figure 14.

+VA CURRENT vs THROUGHPUT

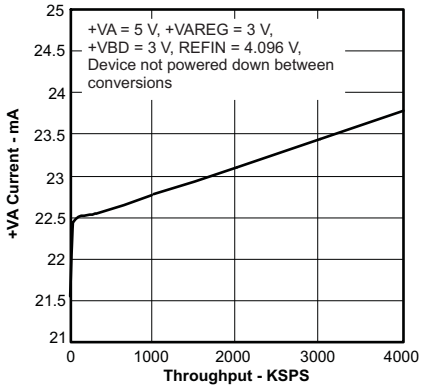


Figure 15.

DIFFERENTIAL NONLINEARITY vs FREE-AIR TEMPERATURE

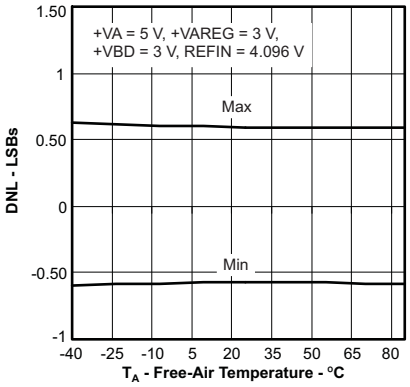


Figure 16.

INTEGRAL NONLINEARITY vs FREE-AIR TEMPERATURE

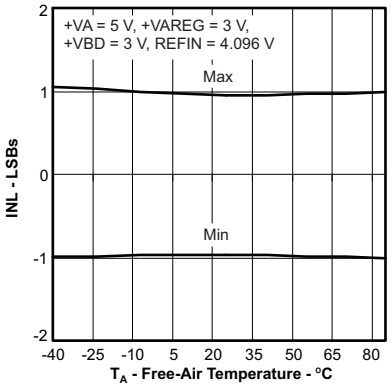


Figure 17.

COMMON-MODE REJECTION RATIO vs FREQUENCY

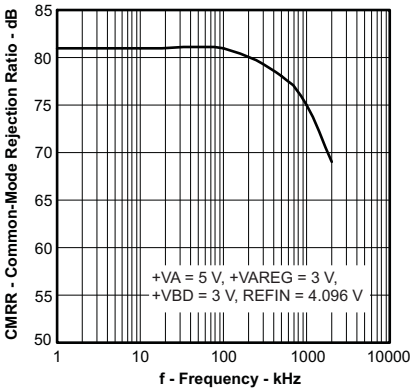


Figure 18.

DNL

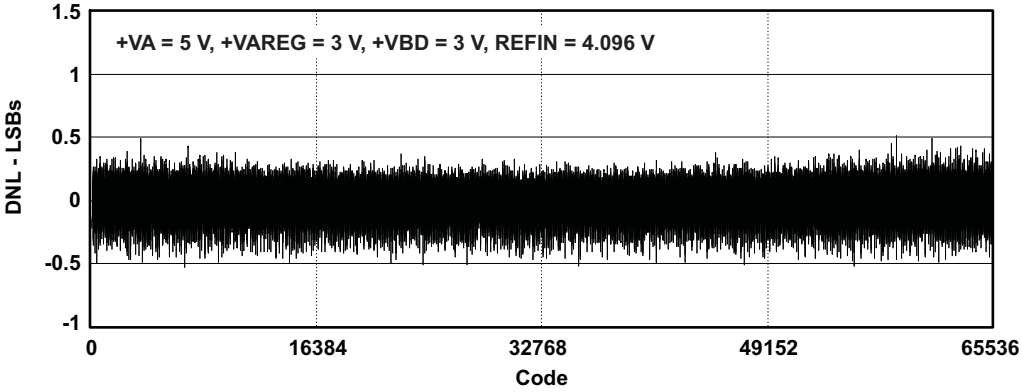


Figure 19.

TYPICAL CHARACTERISTICS (continued)

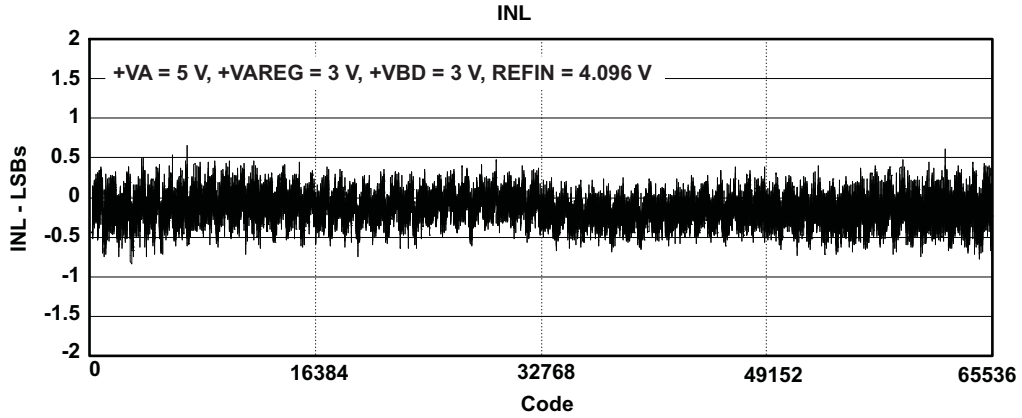


Figure 20.

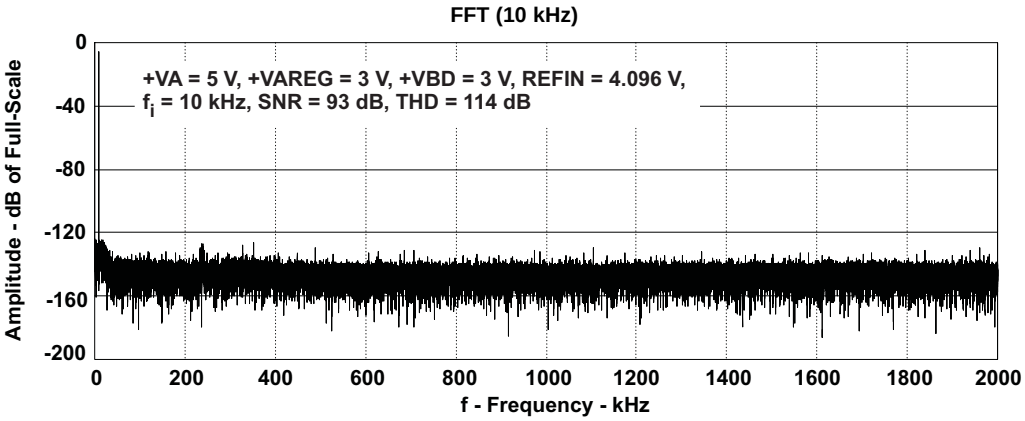


Figure 21.

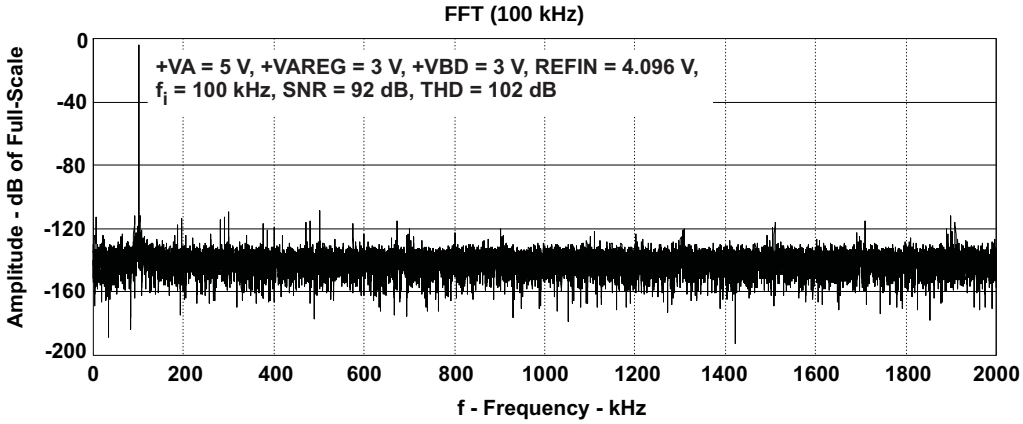


Figure 22.

TYPICAL CHARACTERISTICS (continued)

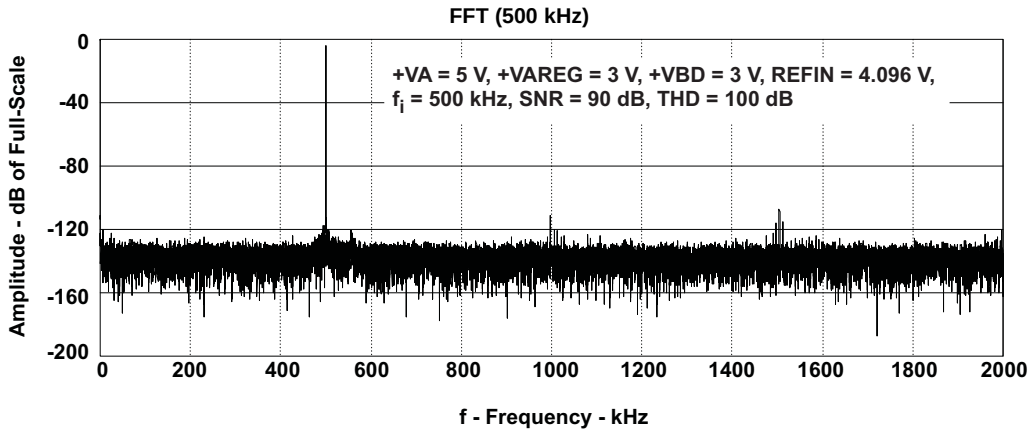
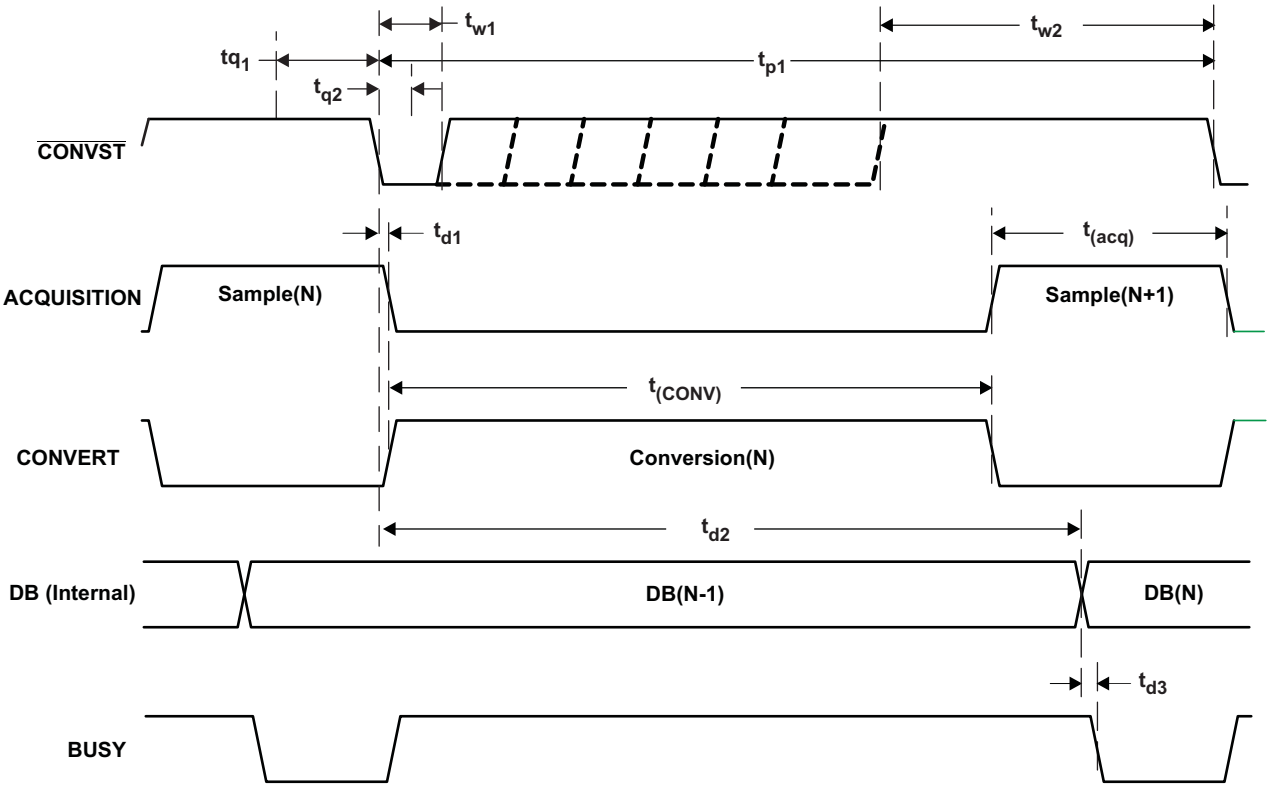


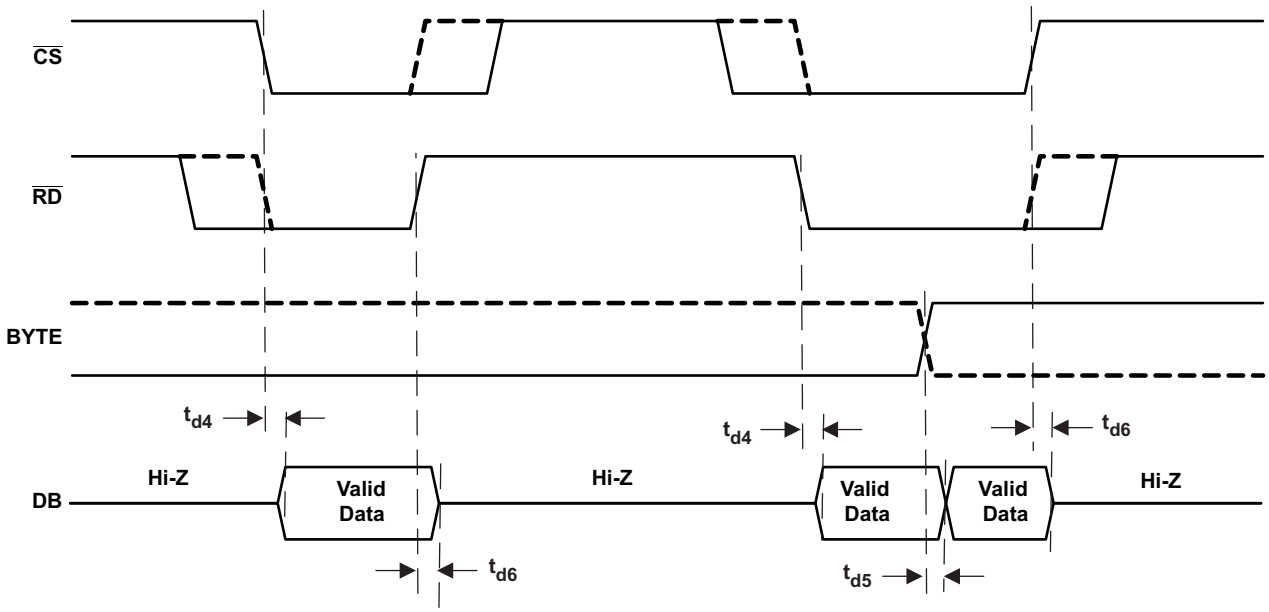
Figure 23.

TIMING DIAGRAMS



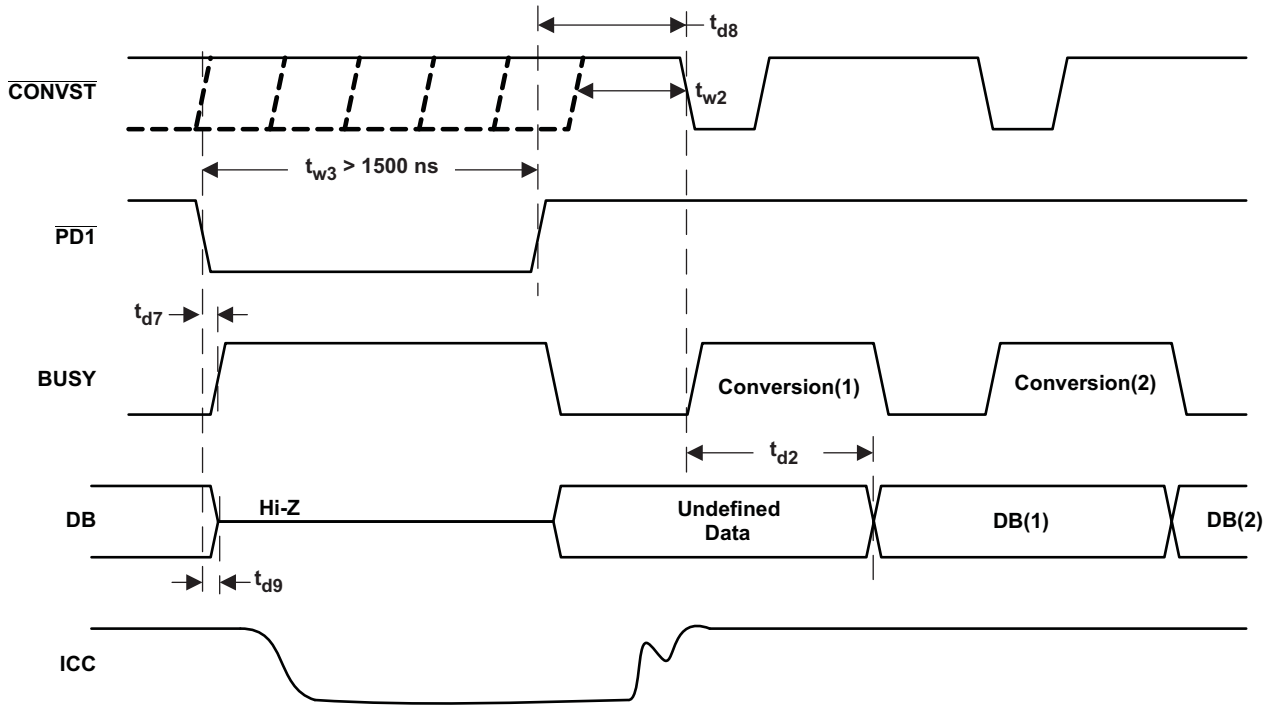
Note: The DB shown here is internal to the device and output on the pins only if and when $\overline{CS}$ and $\overline{RD}$ are both low (after t_{d4} ns). This is shown in Figure 25.

Figure 24. Conversion Control Timing



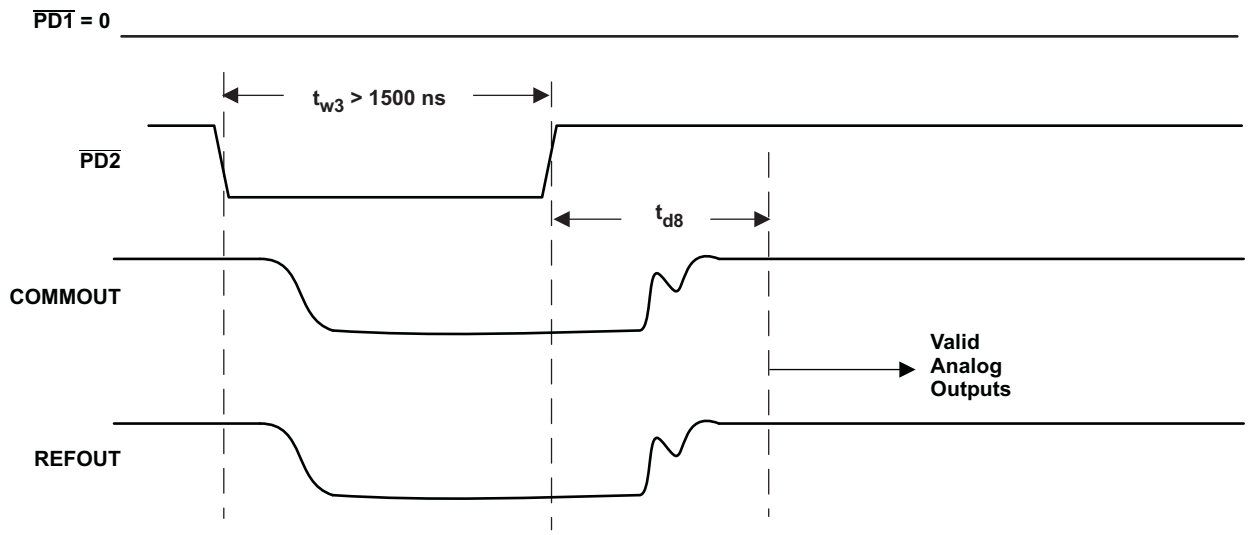
Note: Data is output on the pins only if $\overline{CS}$ and $\overline{RD}$ are both low, t_{d4} ns after this condition is satisfied.

Figure 25. Data Read Timing



Note: Data is valid from the first conversion initiated 5 µs after $\overline{PD1}$ is pulled high.

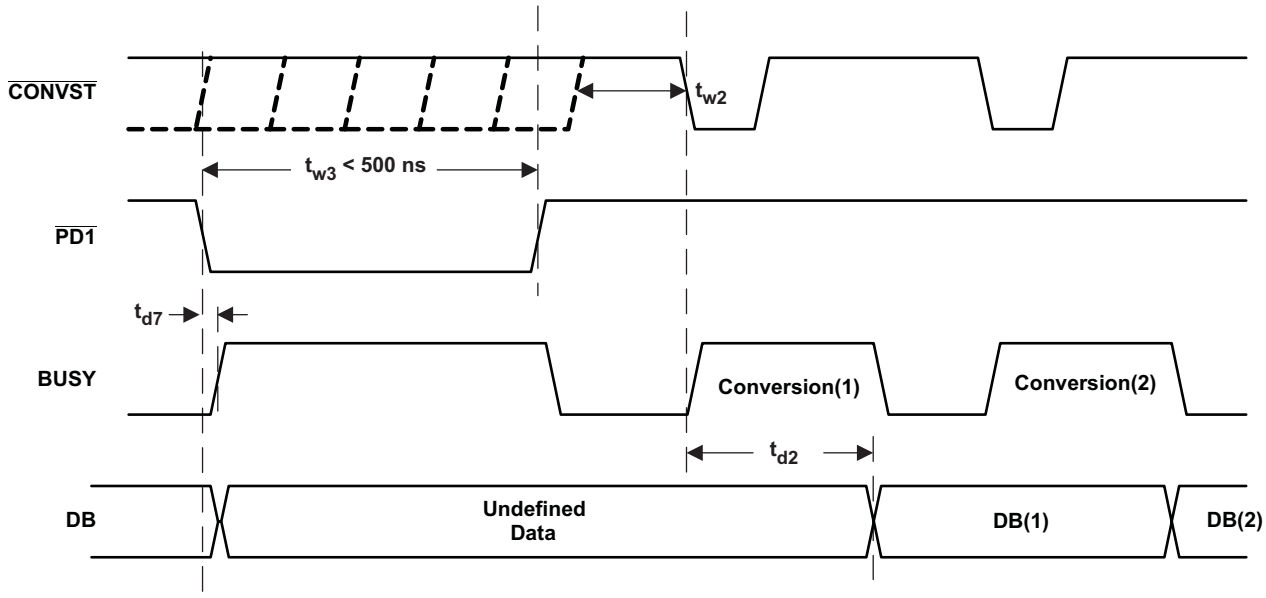
Figure 26. ADC Power-Down Timing



Note: Analog outputs are valid 25 ms after $\overline{PD2}$ is pulled high.

Figure 27. Analog Output Power-Down Timing

RESET TIMING



Note: Data valid from first conversion initiated 100 ns after $\overline{PD1}$ is pulled high.

Figure 28. ADC Reset

PRINCIPLES OF OPERATION

The ADS8422 is a member of a family of high-speed multi-bit successive approximation register (SAR) analog-to-digital converters (ADC). The architecture is based on charge redistribution, which inherently includes a sample/hold function. See Figure 34 for the application circuit for the ADS8422.

The conversion clock is generated internally. The conversion time is a maximum of 180 ns that is capable of sustaining a 4-MHz throughput.

The analog input is provided to two input pins: +IN and -IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

REFERENCE

The ADS8422 has a built-in 4.096-V reference but can operate with an external 4.096-V reference. When internal reference is used, pin 2 (REFOUT) should be connected to pin 1 (REFIN) with a 0.1-µF decoupling capacitor and a 1-µF storage capacitor between pin 2 (REFOUT) and pins 47 and 48 (REFM). The internal reference of the converter is double buffered. If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the capacitors of the CDAC during conversion. Pin 2 (REFOUT) can be left unconnected (floating) if an external reference is used.

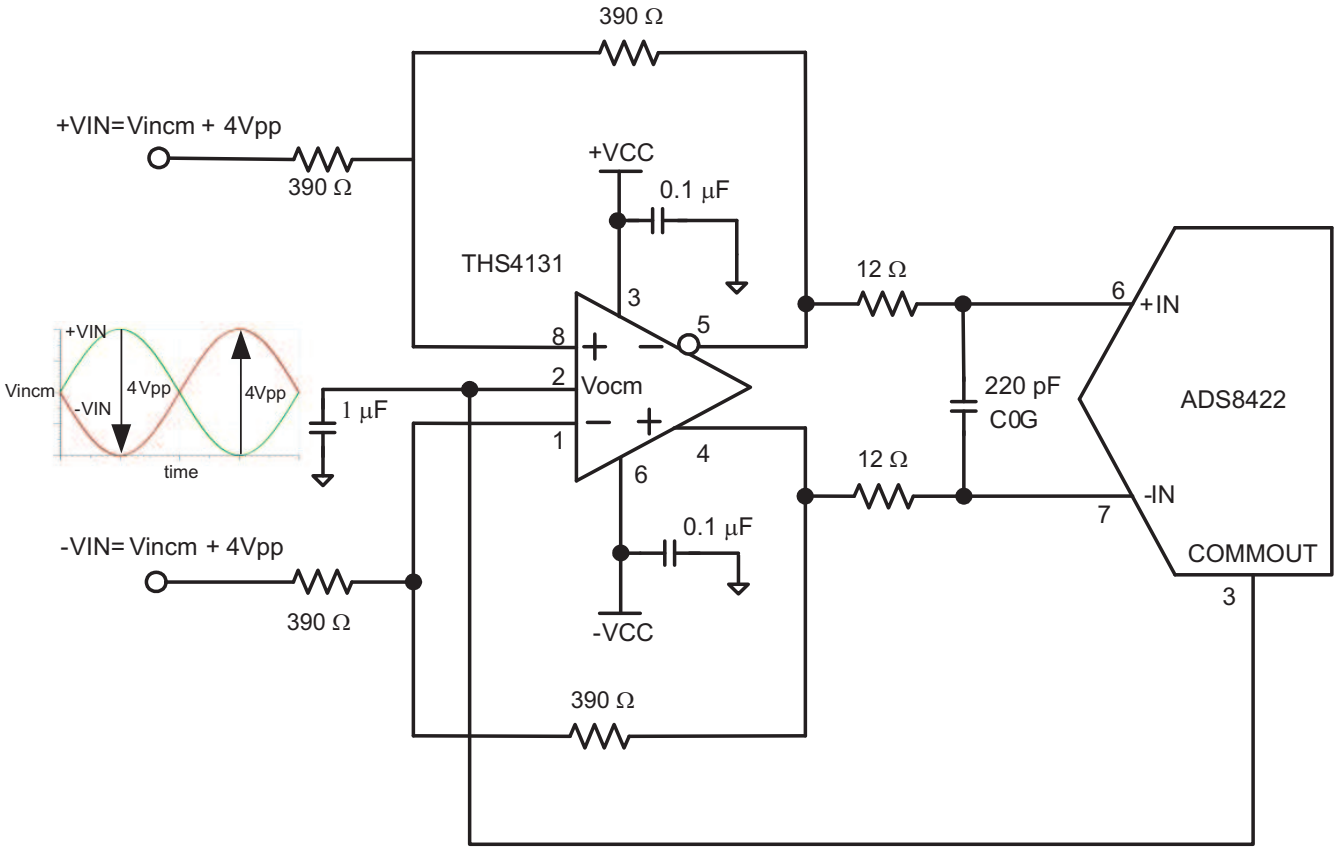
ANALOG INPUT

The ADS8422 has a pseudo-bipolar, fully differential input. When the input is differential, the amplitude of the input equals the difference between +IN and –IN. The peak-to-peak amplitude of each input is V_{REF}. However since the two inputs are 180° out of phase, the peak-to-peak amplitude of the difference voltage [+IN – (–IN)] is equal to $2V_{REF}$. The common-mode input range is from $V_{REF}/2 – 0.2$ V to $V_{REF}/2 + 0.2$ V.

In order to avoid additional external circuitry on the board, the ADS8422 outputs reference input on REFIN divided by 2 on pin 3 (COMMOUT). This voltage can be used to set the common-mode of the output from the input driver.

Figure 29, Figure 30, Figure 31, Figure 32, and Figure 33 show the recommended circuits to interface an analog input signal to the ADS8422.

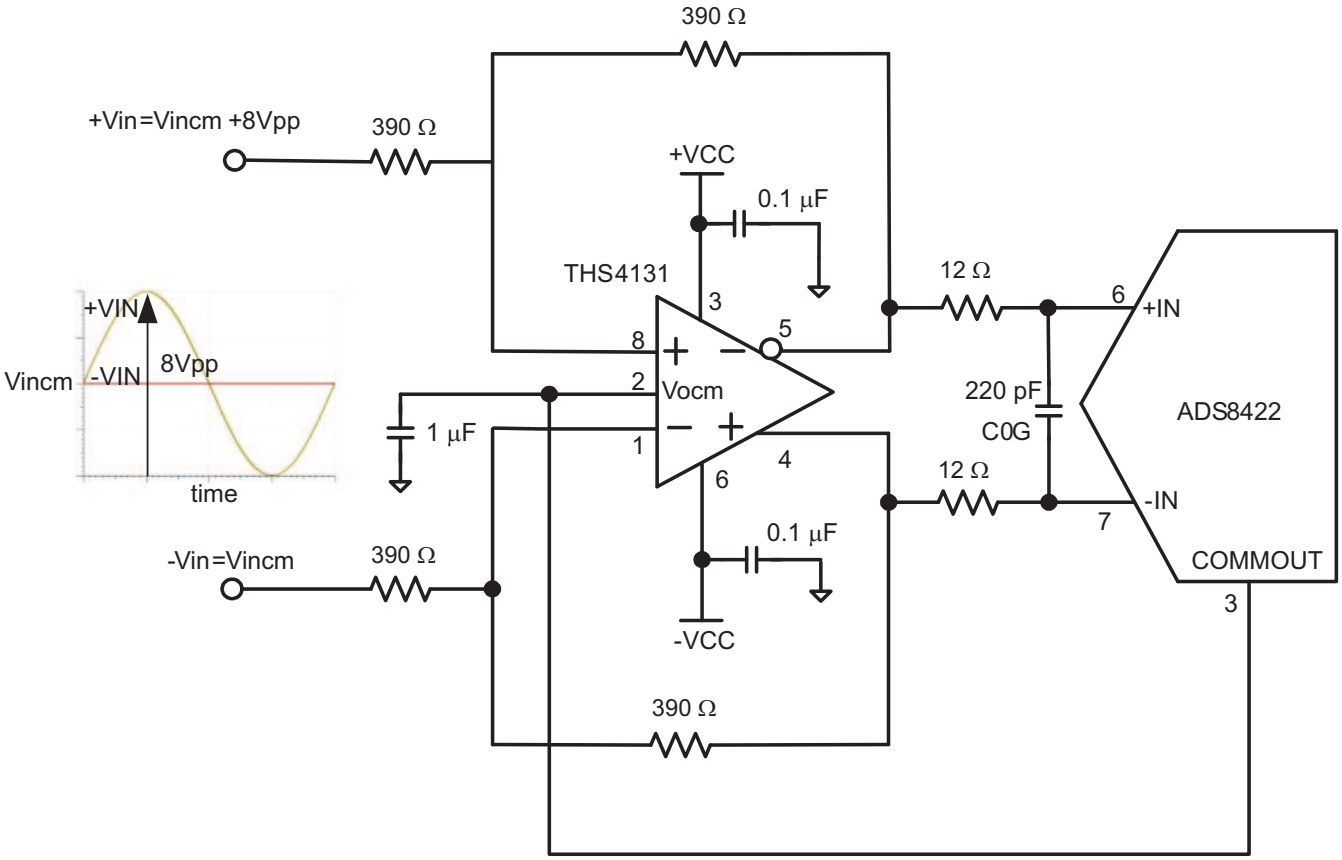
PRINCIPLES OF OPERATION (continued)



A. Input common-mode voltage (Vincm) range is restricted by the amplifier. Refer to the amplifier data sheet for more information. Output common mode of the THS4131 is set by the voltage at pin 2. The COMMOUT pin of the ADS8422 is designed to source pin 2 of the THS4131. However to use this feature both the positive supply and negative supply rails must equal (|-VCC| = |+VCC|), absolutely.

Figure 29. Fully Differential Input Driver Circuit for Unipolar or Bipolar Signals

PRINCIPLES OF OPERATION (continued)



A. Input common-mode voltage (Vincm) range is restricted by the amplifier. Refer to the amplifier data sheet for more information. Output common mode of the THS4131 is set by the voltage at pin 2. The COMMOUT pin of the ADS8422 is designed to source pin 2 of the THS4131. However to use this feature both the positive supply and negative supply rails must equal (|-VCC| = |+VCC|), absolutely.

Figure 30. Single-Ended Input Driving Circuit for When Input is Unipolar or Bipolar

PRINCIPLES OF OPERATION (continued)

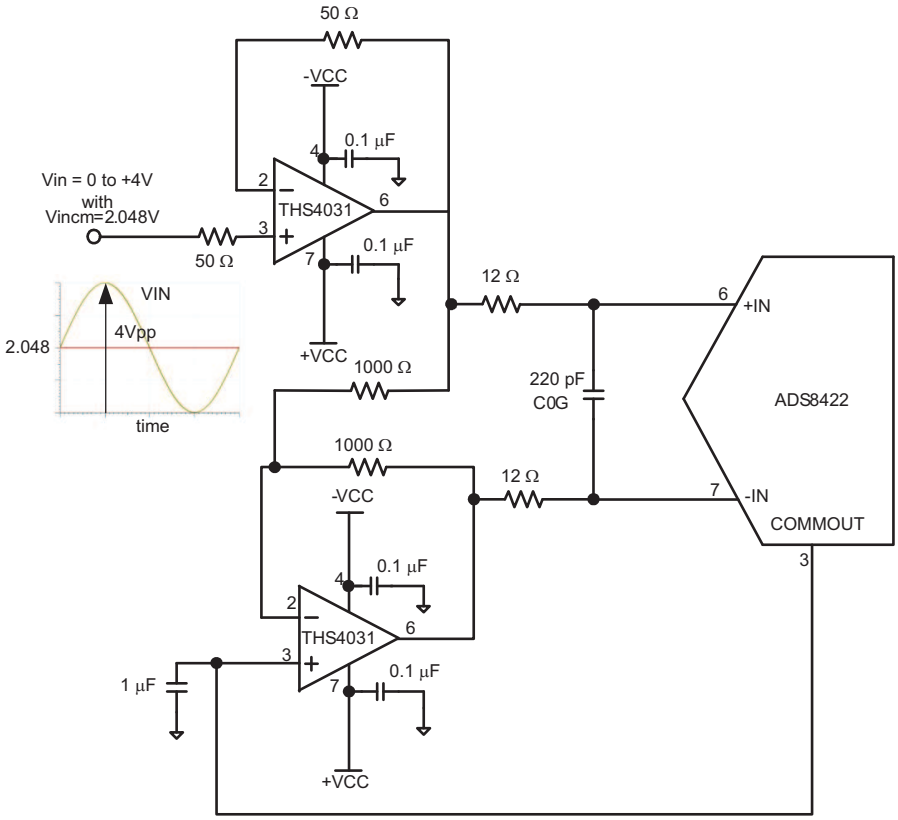
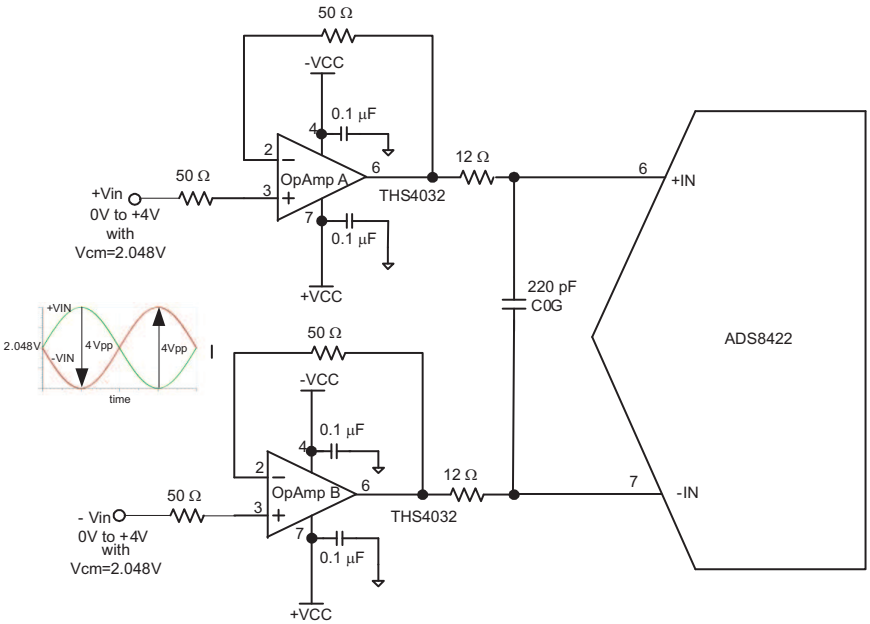


Figure 31. Single-Ended Driving Circuit for When Input is Single-Ended Unipolar and has Common-Mode of 2.048 V



A. This circuit is used to specify ADS8422 performance parameters listed in the data sheet.

Figure 32. Driver Circuit for When Input is Fully Differential Riding on Common-Mode of 2.048 V

PRINCIPLES OF OPERATION (continued)

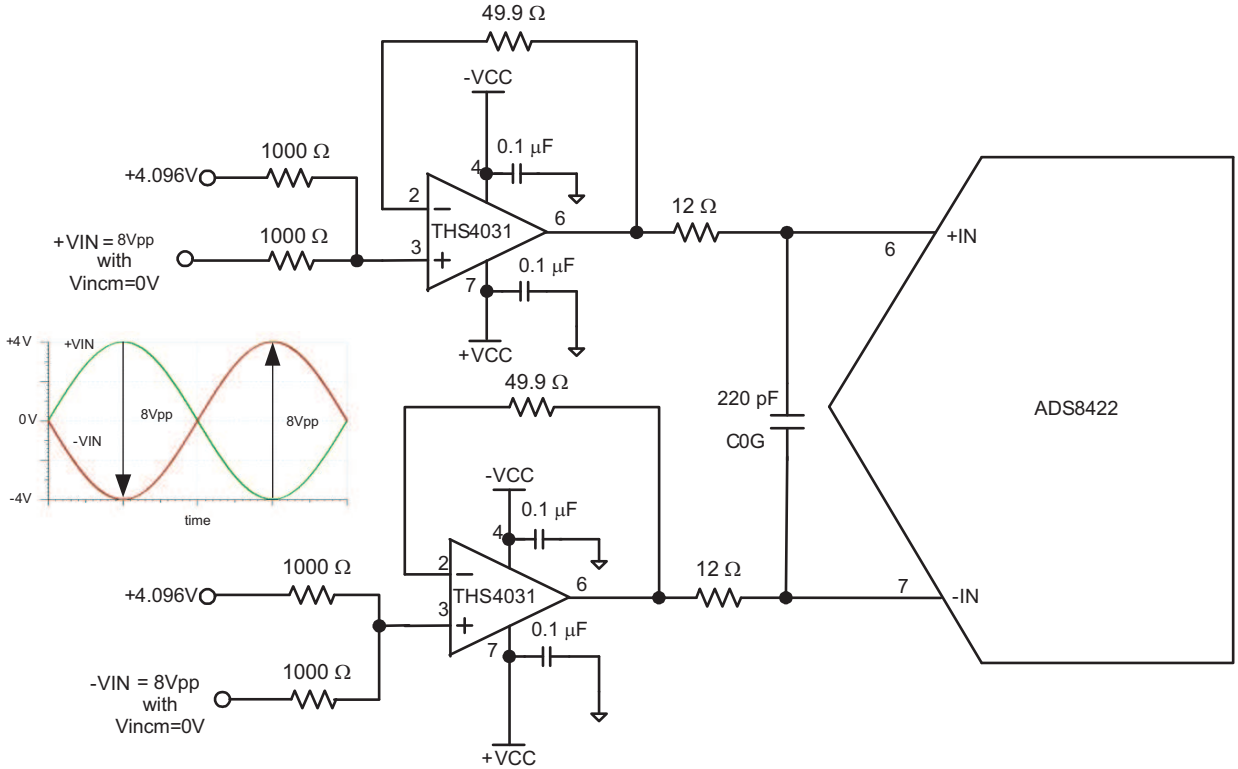


Figure 33. Driver Circuit for Bipolar Fully Differential Input Signals with 0-V Common-Mode

The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS8422 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (30 pF) to a 16-bit settling level within the 70 ns acquisition time of the device. When the converter goes into hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, both -IN and +IN inputs should be within the limits specified. Outside of these ranges, the converter linearity may not meet specifications. To minimize noise, low bandwidth input signals with low pass filters should be used.

Care should be taken to ensure that the output impedances of the sources driving the +IN and –IN inputs are matched. If this is not observed, the two inputs could have different settling times. This may result in offset error, gain error, and linearity error which change with temperature and input voltage.

When the converter enters hold mode, the voltage difference between the +IN and -IN inputs is captured on the internal capacitor array.

DIGITAL INTERFACE

Timing and Control

See the timing diagrams for detailed information on timing signals and their requirements.

The ADS8422 uses an internal oscillator generated clock which controls the conversion rate and in turn the throughput of the converter. No external clock input is required.

PRINCIPLES OF OPERATION (continued)

Conversions are initiated by bringing the $\overline{\text{CONVST}}$ pin low for a minimum of 20 ns (after the 20 ns minimum requirement has been met, the $\overline{\text{CONVST}}$ pin can be brought high). The converter switches from sample to hold mode on the falling edge of the $\overline{\text{CONVST}}$ command. A clean and low jitter falling edge of this signal is important to the performance of the converter. The BUSY pin is brought high immediately following $\overline{\text{CONVST}}$ going low. BUSY stays high through the conversion process and returns low when the conversion has ended and data is available on the DB pins. Once the conversion is started, it cannot be stopped except with an asynchronous $\overline{\text{RESET}}$ (or a logical $\overline{\text{PD1}}$).

If $\overline{\text{CONVST}}$ is detected high at the end of conversion, the device immediately enters sampling mode and the analog input is connected to the CDAC. Otherwise, the CDAC is connected to the analog input only when $\overline{\text{CONVST}}$ goes high. The high duration of $\overline{\text{CONVST}}$ should be at least 100 ns. There is no maximum high pulse duration specification for $\overline{\text{CONVST}}$.

Reading Data

The ADS8422 outputs full parallel data in 2's complement format as shown in Table 1. The parallel output is active when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are both low. There is a minimal quiet zone requirement around the falling edge of $\overline{\text{CONVST}}$. This is 30 ns prior to the falling edge of $\overline{\text{CONVST}}$ and 10 ns after the falling edge. No data read should be attempted within this zone. Any other combination of $\overline{\text{CS}}$ and $\overline{\text{RD}}$ three-states the parallel output. BYTE is used for multi-word read operation. BYTE is used whenever lower bits on the bus are output on the higher byte of the bus. Refer to Table 1 for ideal output codes.

Table 1. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT 2'S COMPLIMENT	
Full scale range	$2V_{ref}$		
Least significant bit (LSB)	$2V_{ref}$)/65536	BINARY CODE	HEX CODE
+Full scale	$(+V_{ref})$ –	0111 1111 1111 1111	7FFF
Midscale	0 V	0000 0000 0000 0000	0000
Midscale – 1 LSB	0 V –	1111 1111 1111 1111	FFFF
-Full scale	$-V_{ref}$+	1000 0000 0000 0000	8000

The output data can be read as a full 16-bit word on pins DB15 – DB0 (MSB-LSB) if BYTE is low.

The result may also be read on an 8-bit bus for convenience. This is done by using only pins DB15-DB8. In this case two reads are necessary: the first as before, leaving BYTE low and reading the 8 most significant bits on pins DB15-DB8, then bringing BYTE high. When BYTE is high, the low bits (D7-D0) appear on pins DB15-DB8.

These multi-word read operations can be performed with a multiple active (toggling) $\overline{\text{RD}}$ signal or with the $\overline{\text{RD}}$ signal tied low for simplicity.

Table 2. Conversion Data Read Out

BYTE	DATA READ OUT	
	PINS DB15–DB8	PINS DB7–DB0
High	D7 - D0	All One's
Low	D15 - D8	D7 - D0

RESET

$\overline{\text{RESET}}/\overline{\text{PD1}}$ is an asynchronous active low input signal. Maximum $\overline{\text{RESET}}/\overline{\text{PD1}}$ low time is 0.5 µs to avoid ADC powerdown. Current conversion is aborted no later than 20 ns after the converter is in reset mode. The converter returns to normal operation mode no later than 20 ns after the $\overline{\text{RESET}}/\overline{\text{PD1}}$ input is brought high (see Figure 28).

The converter provides two power saving options: ADC powerdown (using pin 38, $\overline{\text{PD1}}$) and analog output powerdown ($\overline{\text{PD2}}$).

ADC powerdown is activated by asserting $\overline{PD1}$ to 0 for longer than 1.5 µs. If the signal $\overline{PD1}$ is asserted 0 for less than 0.5 µs, the ADC is only reset and any ongoing conversion aborted. See Figure 26. ADC operation can be resumed from ADC powerdown by de-asserting the $\overline{PD1}$ pin. In ADC power-down mode, the analog outputs from the ADC(COMMOUT, REFOUT) are not powered down thereby reducing the power-on time.

Full chip power-down is activated by turning off the power supply or by asserting both, $\overline{PD1}$ = 0 and $\overline{PD2}$ = 0 for longer than 1.5 µs (see Figure 27). In this mode, even the analog outputs of the ADC (COMMOUT, REFOUT) are powered down thereby giving maximum power saving. Device operation can be resumed from full chip power-down by turning on the power supply or by deasserting both, $\overline{PD1}$ = 1 and $\overline{PD2}$ = 1.

Table 3. Effects of $\overline{RESET}$, $\overline{PD1}$, and $\overline{PD2}$

COMMAND	APPLICATION TIME	POWER WHEN APPLIED	RESUME TIME
$\overline{RESET}/\overline{PD1}$ = 0	20 ns	No change	20 ns
$\overline{PD1}$ = 0, $\overline{PD2}$ = 1	1.5 µs	17mW	5 µs
$\overline{PD1}$ = $\overline{PD2}$ = 0	1.5 µs	40 µW	25 ms
$\overline{PD1}$ = 1, $\overline{PD2}$ = 0	Reserved – Do not use this combination		

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8422 circuitry.

As the ADS8422 offers single-supply operation, it is often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-clock SAR converter, there are n *windows* in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices. The 50 ns period before BUSY falls should be kept free of supply glitches.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event.

On average, the ADS8422 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1-µF bypass capacitor is recommended from pin 1 directly to REFM (pin 48). REFM and AGND should be shorted on the same ground plane underneath the device.

The AGND, BDGND, and AGND pins should be connected to a clean ground point. In all cases, this should be the *analog* ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

As with the AGND connections, +VA and +VAREG should be connected to their respective power supply planes or traces that are separate from the connection for digital logic, until they are connected at the power entry point. Power to the ADS8422 should be clean and well bypassed. A 0.1-µF ceramic bypass capacitor should be placed as close to the device as possible. See Table 4 for capacitor placement. In addition, a 1-µF to 10-µF capacitor is recommended. In some situations, additional bypassing may be required, such as a 100-µF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors — all designed to essentially low-pass filter the +5-V supply, thus removing the high frequency noise.

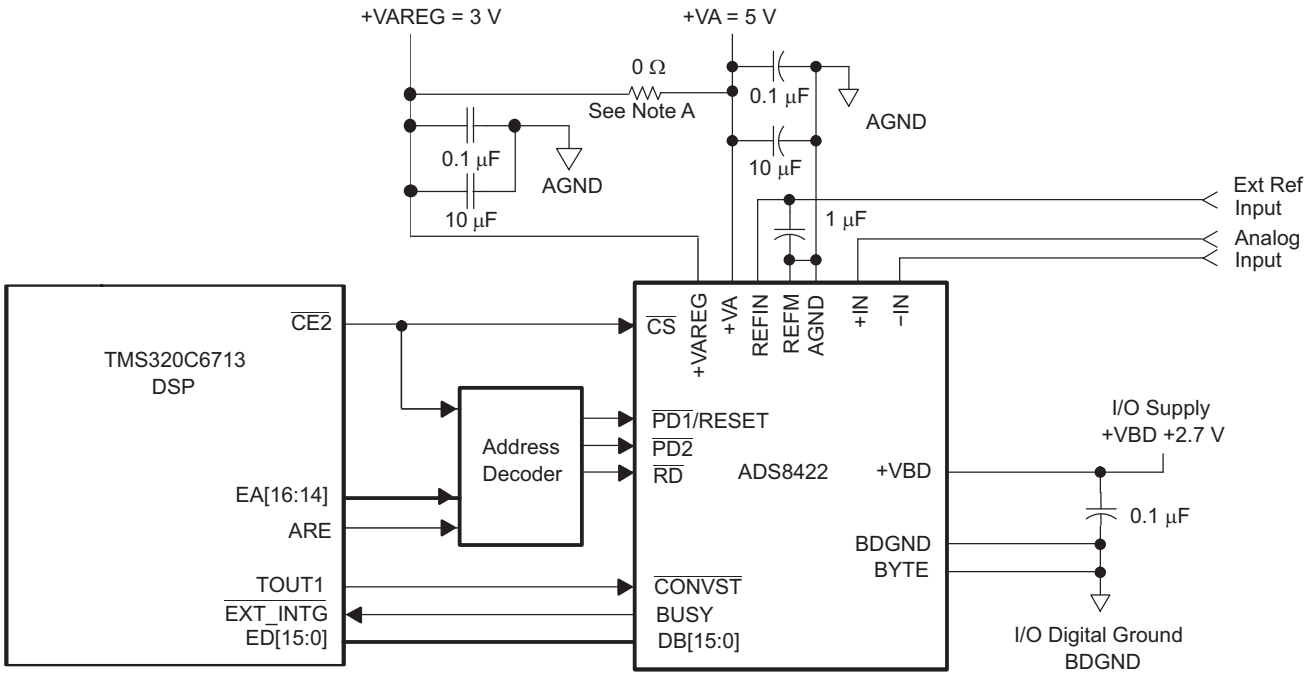
Table 4. Power Supply Decoupling Capacitor Placement

POWER SUPPLY PLANE	CONVERTER ANALOG SIDE	CONVERTER DIGITAL SIDE
SUPPLY PINS		
Pin pairs that require shortest path to decoupling capacitors	(4,5), (9,8), (10,12), (13,15), (43,44), (46,45)	(24,25), (34,35)

APPLICATION INFORMATION

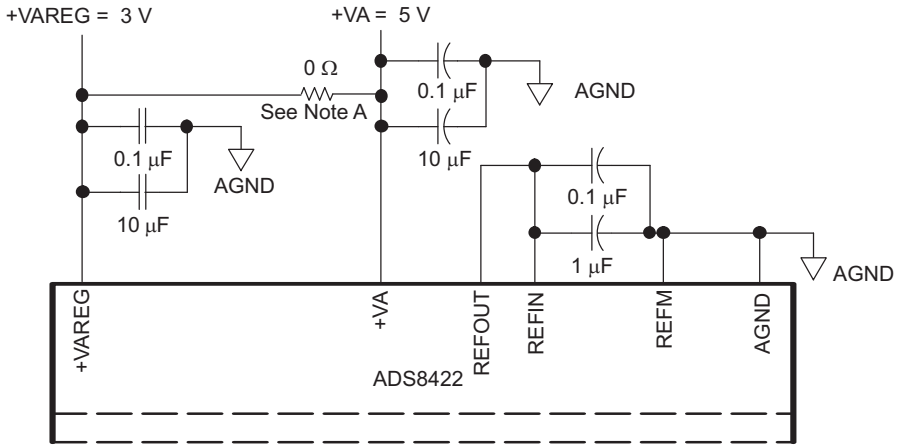
ADS8422 TO A HIGH PERFORMANCE DSP INTERFACE

Figure 34 shows a parallel interface between the ADS8422 and a Texas instruments high performance DSP such as the TMS320C6713 using the full 16-bit bus. The ADS8422 is mapped onto the $\overline{CE2}$ memory space of the TMS320C6713 DSP. The read and reset signals are generated by using a 3-to-8 decoder. A read operation from the address 0xA000C000 generates a pulse on the $\overline{RD}$ pin of the data converter, wheras a read operation form word address 0xA0014000 generates a pulse on the $\overline{RESET}$/$\overline{PD1}$ pin. The $\overline{CE2}$ signal of the DSP acts as $\overline{CS}$ (chip select) for the converter. As the TMS320C6713 features a 32-bit external memory interface, the BYTE input of the converter can be tied permanently low, disabling the foldback of the data bus. The BUSY signal of the ADS8422 is appiled to the $\overline{EXT_INT6}$ interrupt input of the DSP, enabling the EDMA controller to react on the falling edge of this signal and to collect the conversion result. The TOUT1 (timer out 1) pin of the TMS320C6713 is used to source the $\overline{CONVST}$ signal of the converter.



A. This resistor (0 Ω) can be installed to use the same 5-V supply.

Figure 34. ADS8422 Application Circuitry



A. This resistor (0 Ω) can be installed to use the same 5-V supply.

Figure 35. ADS8422 Using Internal Reference

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8422IBPFBR	ACTIVE	TQFP	PFB	48	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8422I B	Samples
ADS8422IBPFBT	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8422I B	Samples
ADS8422IBPFBTG4	ACTIVE	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8422I B	Samples
ADS8422IPFBR	ACTIVE	TQFP	PFB	48	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8422I	Samples
ADS8422IPFBRG4	ACTIVE	TQFP	PFB	48	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8422I	Samples
ADS8422IPFBT	NRND	TQFP	PFB	48	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 8422I	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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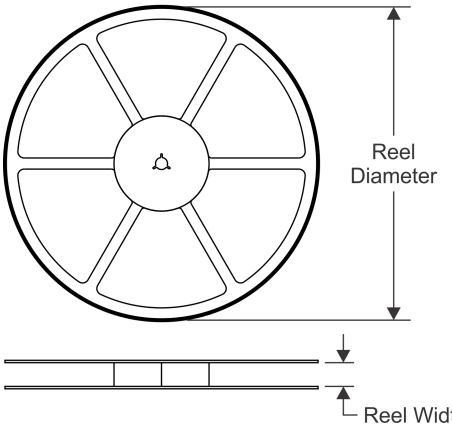
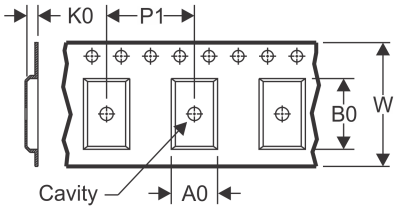
TAPE AND REEL INFORMATION

REEL DIMENSIONS

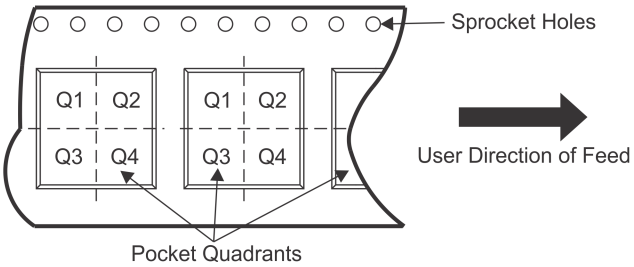


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

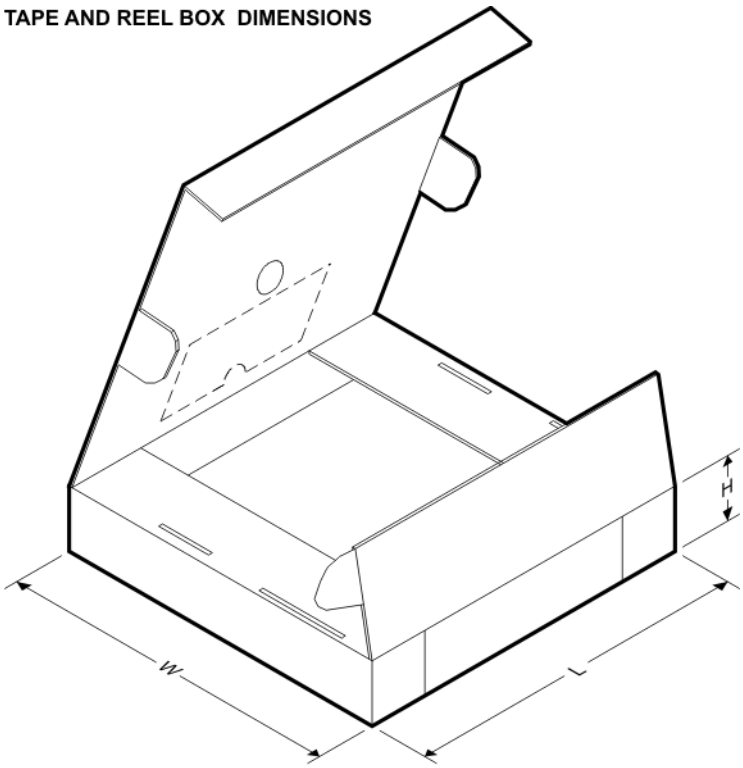
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8422IBPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
ADS8422IBPFBT	TQFP	PFB	48	250	180.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
ADS8422IPFBR	TQFP	PFB	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
ADS8422IPFBT	TQFP	PFB	48	250	180.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

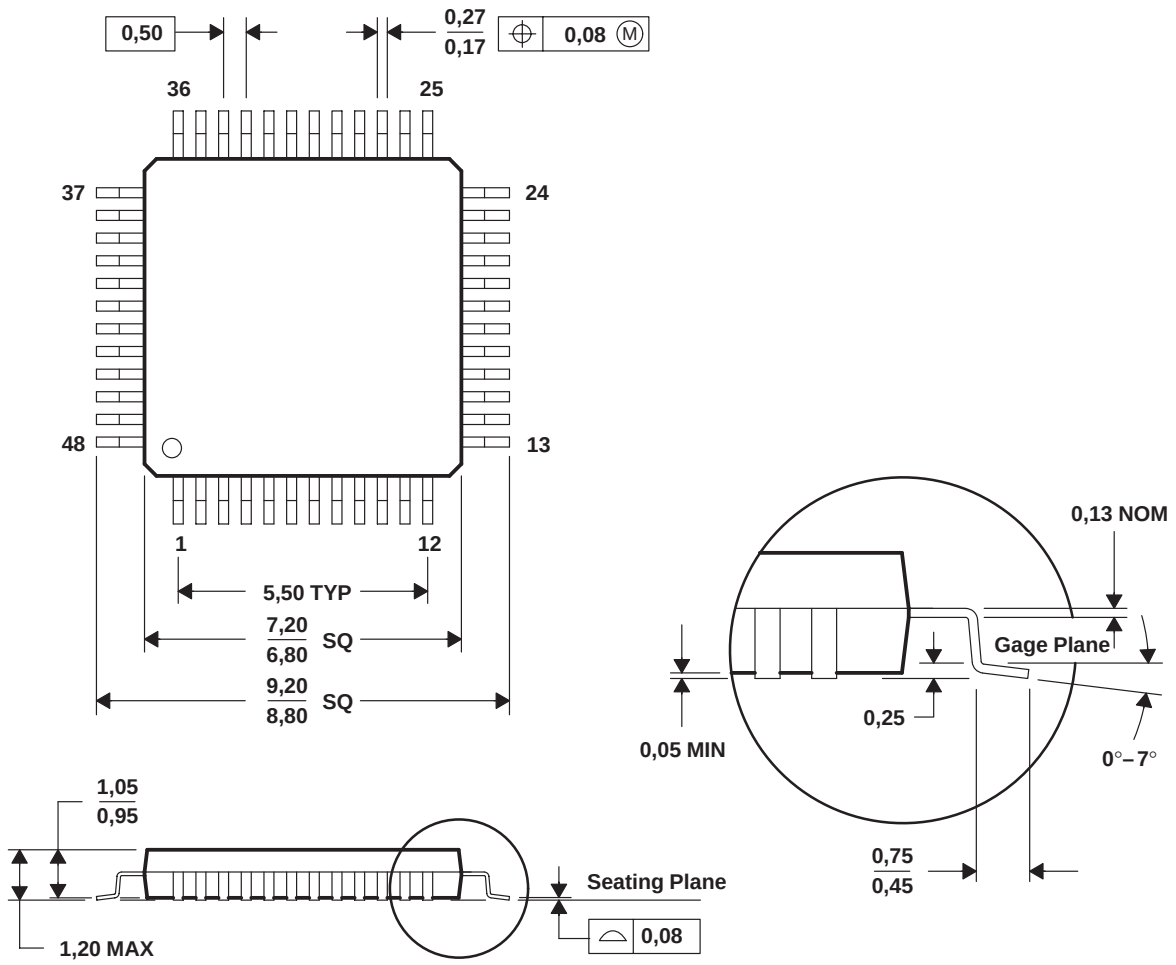
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

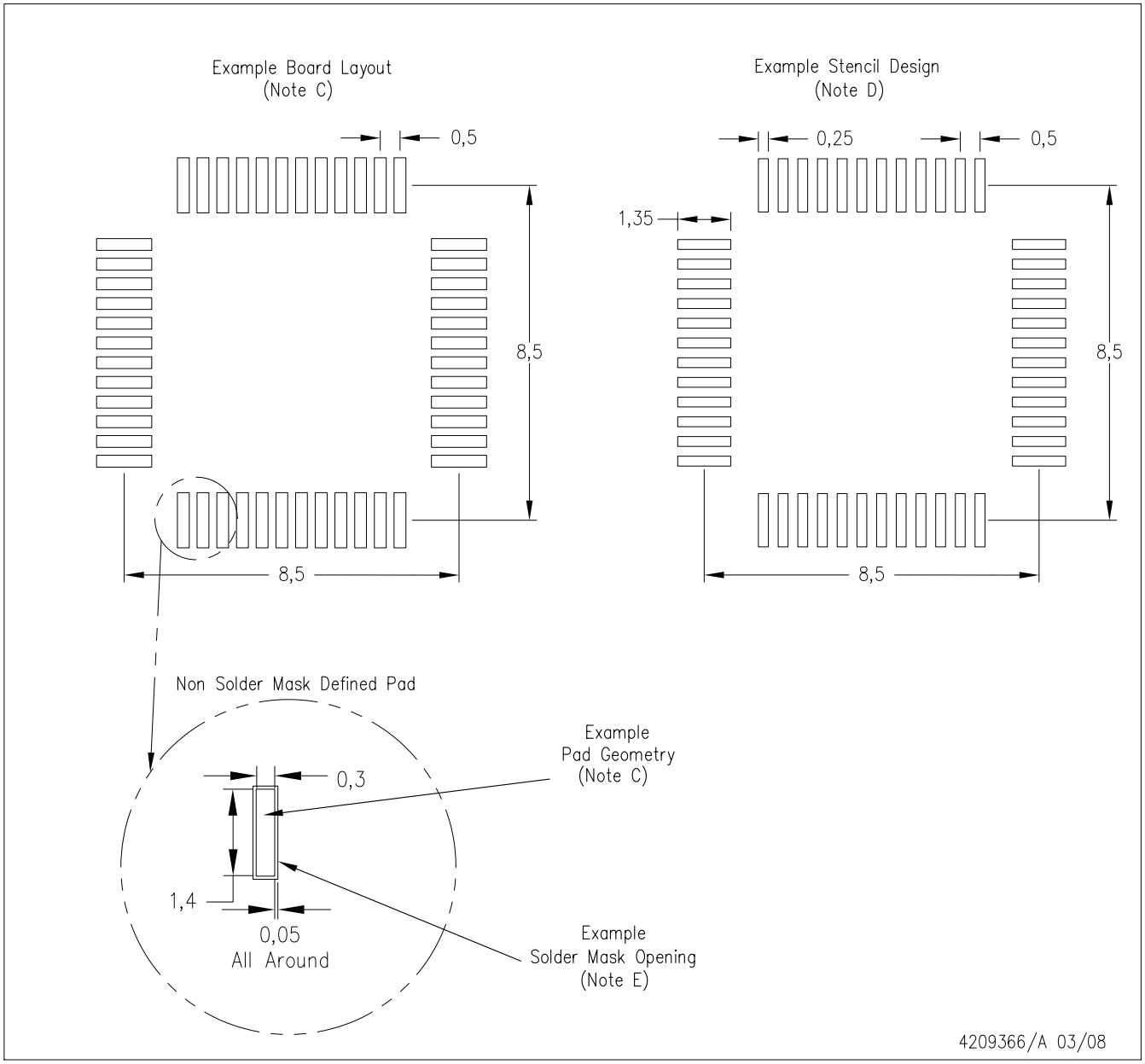
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8422IBPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
ADS8422IBPFBT	TQFP	PFB	48	250	213.0	191.0	55.0
ADS8422IPFBR	TQFP	PFB	48	1000	350.0	350.0	43.0
ADS8422IPFBT	TQFP	PFB	48	250	213.0	191.0	55.0

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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